IN THE TITLE:

The title has been amended herein. Pursuant to 37 C.F.R. §§ 1.121 and 1.125 (as amended to date), please enter the title as amended.

INTERPOSER WITH A LATERAL ~~RECESSED~~ RECESS IN A SLOT TO FACILITATE CONNECTION OF INTERMEDIATE CONDUCTIVE ELEMENTS TO BOND PADS OF A SEMICONDUCTOR DIE WITH WHICH THE INTERPOSER IS ASSEMBLED

IN THE SPECIFICATION:

Please replace paragraph number [0004] with the following rewritten paragraph:

[0004] One example of such a technology is the so-called ~~"flip-chip",~~ "flip-chip," or controlled collapse chip connection (C-4), technology. In flip-chip technology, the bond pads or contact pads of a semiconductor device are arranged in an array over a major surface of the semiconductor device. Flip-chip techniques are applicable to both bare and packaged semiconductor devices. A packaged flip-chip type semiconductor device, which typically has a "ball grid array" (BGA) connection pattern, typically includes a semiconductor die and a substrate element, which is typically termed an ~~"interposer".~~ "interposer." The interposer may be disposed over either the backside of the semiconductor die or the front (active) surface thereof.

Please replace paragraph number [0010] with the following rewritten paragraph:

[0010] Another approach to reducing the sizes of assemblies of semiconductor devices and carrier substrates has been to reduce the amount of ~~"real estate",~~ "real estate," or surface area, upon a carrier substrate that is consumed by individual semiconductor device packages. This is typically done by reducing the dimensions of the semiconductor device packages along a plane that is parallel to a plane of the substrate upon which the semiconductor device packages are to be carried. As a result of ever-decreasing package dimensions, the so-called "chip-scale package" (CSP) has been developed. The dimensions of the outer peripheries of chip-scale packages are typically substantially the same as or only slightly larger than the corresponding dimensions of the outer peripheries of the semiconductor dice that are used in chip-scale packages.

Please replace paragraph number [0029] with the following rewritten paragraph:

[0029] As shown, the interposer 30 includes an aperture, or slot 14, formed therethrough for exposing the bond pads 12 of a semiconductor device 20 over which the interposer 30 is to be positioned. The slot 14 has a first end 15 that is configured to extend laterally beyond an outer periphery 21 of the semiconductor die 20 when the interposer 30 and

semiconductor die 20 are properly oriented with respect to one another. As the first end 15 of the slot 14 is configured to extend beyond the outer periphery 21 of a semiconductor die 20 to which the interposer 30 is attached, the first end 15 does not restrict the flow of encapsulant material being introduced into the slot 14 and is, therefore, also referred to herein as a "nonmold flow restriction ~~end"~~. end."